AND8376/D

AMIS−30660/42000 − Topology Aspects of a High−Speed CAN Bus

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APPLICATION NOTE

Introduction

AMIS−30660, together with AMIS−42000, is a family of high speed CAN transceiver products intended for automotive and industrial applications. Although individual members of the product family differ in some aspects − operation modes, additional features, single−channel bus versus bus−repeater etc. − they all incorporate high−speed CAN transceiver(s) compliant with ISO11898 norm. The transceiver functional blocks throughout the product family share the same set of limitations which have to be considered when designing the topology of the CAN bus which they interface.

A CAN bus topology is determined by the number of nodes, maximum allowed bus length and the maximum allowed length of unterminated stubs connected to the main bus line. These topology parameters are mainly defined by:

1. The delay of the line and the loop delay of the nodes (loop delay is the sum of the receiver delay, the transmitter delay and the delays of the interface lines between the transceiver and the CAN controller)
2. The signal amplitude drop due to the non−zero bus wire resistance and the finite input resistance of the nodes
3. Differences of oscillator frequency between nodes

This application note deals with points 1 and 2, whereas point 3 − the oscillator frequency tolerance − is not considered.

After a definition of CAN bit timing related terms and parameters in the “Definition of CAN Bit Timing” section, the application note addresses the following questions in individual chapters:

1. What is the maximum bus length if the bit timing parameters are known?
2. What is the maximum length of unterminated stubs if the bit timing parameters are known?
3. What is the maximum bus length for a given number of nodes which still guarantees sufficient signal amplitude?
4. What is the maximum number of nodes which can be driven by the given CAN transceiver?

Although these points are analyzed separately, all of them should be considered and the resulting conditions should be fulfilled simultaneously in order to achieve a correct bus topology.

DEFINITION OF CAN BIT TIMING

Parameter Definition

This paragraph gives an abbreviated definition of parameters related to the CAN bit timing which will be used later in relation with the bus topology aspects.

A CAN bus system uses a nominal bit rate f_{nbr} (in bits per second) which is uniform throughout the network. To each bit corresponds an interval of time:

$$T_{bit} = \frac{1}{f_{nbr}}$$

As defined in detail in [1], each node in a CAN network has to perform frequent “hard synchronization” and “re−synchronization” in order to ensure correct data processing according the CAN protocol. For the purpose of the synchronization, the CAN controller regards each bit period as being split to several segments as shown in Figure 1.

The time in a CAN node is referred to a CAN system clock, the period of which is called “time quantum” T_Q. ISO CAN norm [1] requires that each bit period is split to 8−25 time quanta, i.e. that the CAN system clock is 8−25 times faster than the nominal bit rate. The CAN system clock controls the bit timing and sampling of the bus state. The CAN system clock is derived from the node local oscillator by means of a prescaler. The choice of the local oscillator frequency and of the time quantum value derived from the local oscillator is a task of the CAN system design.

January, 2009 − Rev. 2

Publication Order Number:
AND8376/D

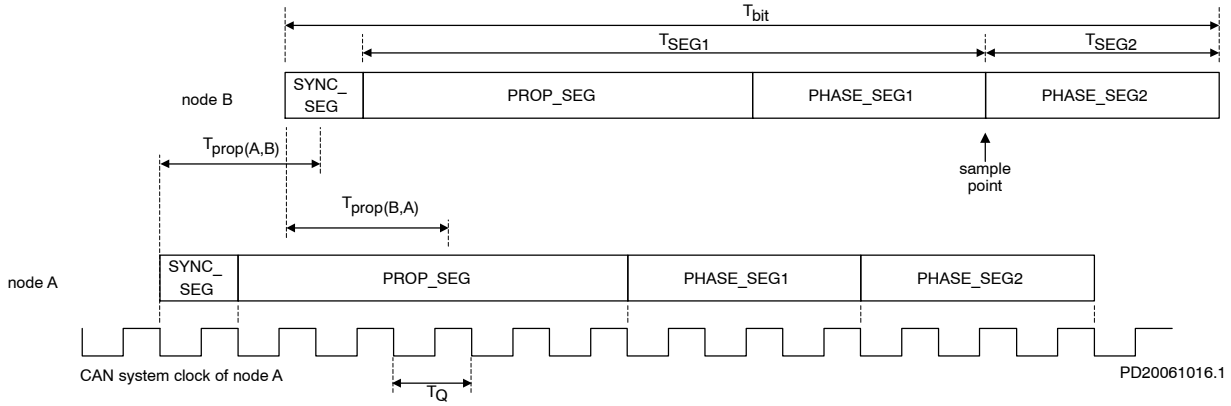

Figure 1. CAN Bit Timing

Each bit period begins with a SYNC_SEG, the duration of which is fixed to one period of the CAN system clock. Transmitting node begins to drive the bus at the beginning of the SYNC_SEG, whereas a correctly synchronized receiving node expects every edge on the bus arriving during SYNC_SEG.

The bit period continues with a PROP_SEG, a period fixed by the CAN system design to 1−8 time quanta. It's the minimum time a receiver will wait before accepting a valid bus value sample. Following segments PHASE_SEG1 and PHASE_SEG2 are periods of time which are adapted during the "re−synchronization" in order to move the "sample point". The maximum allowed one−time modification of the PHASE_SEG1 or PHASE_SEG2 is referred to as SJW, or "synchronization jump width".

Some definitions or software packages might use an alternative set of terms, splitting the bit period to SYNC_SEG, SEG1 and SEG2 (see Figure 1), where:

$$T_{SEG1} = T_{PROP\_SEG} + T_{PHASE\_SEG1}$$
$$T_{SEG2} = T_{PHASE\_SEG2}$$

However, the CAN timing remains identical, as these definitions are purely formal.

The bus state detected at the "sample point" is accepted by the receiving node as the logical value valid for the current bit period. Under the worst case conditions, by modifying the duration of PHASE_SEG1 and PHASE_SEG2, the sample point might arrive as early as immediately after the PROP_SEG part of the bit period.

Maximum Bus Length in Function of Maximum Bus Line Delay

To identify the permissible maximum line delay, the node relation in Figure 1 has to be considered. During an "acknowledge" field, the transmitting node (node A) transmits a recessive bit but expects a dominant bit being transmitted by other nodes (node B in the figure). For the "acknowledge" field to be correctly received, node A has to sample "dominant" at his sample point.

As explained in "Definition of CAN Bit Timing" section, the sample point might arrive as early as immediately after the PROP_SEG period, which must thus accommodate for all propagation delays between node A and node B:

$$T_{PROP\_SEG} \geq T_{PROP(A,B)} + T_{PROP(B,A)}$$

The propagation delays are the total delays between the CAN controller interface of node A (pins TxD_A and RxD_A) and the CAN controller interface of node B (pins TxD_B and RxD_B) and their components are shown in Figure 2.

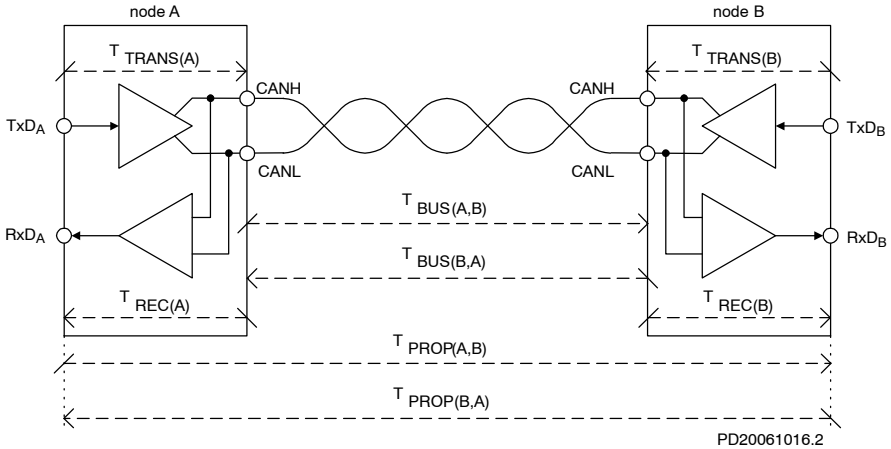

Figure 2. Components of the CAN Bus Delay

The delays can be expressed as follows:

$$T_{PROP(A,B)} = T_{TRANS(A)} + T_{BUS(A,B)} + T_{REC(B)}$$
$$T_{PROP(B,A)} = T_{TRANS(B)} + T_{BUS(B,A)} + T_{REC(A)}$$

Where:

$T_{BUS(X,Y)}$ is the proper bus line delay from node X to node Y.

$T_{TRANS(X)}$ and $T_{REC(X)}$ are delays of node X transmitter and receiver parts, respectively.

The sum of $T_{TRANS(X)}$ and $T_{REC(X)}$ can be found in specifications of CAN transceivers as “propagation delay TxD to RxD”.

The bus line is then limited by the following formula:

$$L_{BUS\_MAX\_DEL} = \frac{\left(\frac{T_{PROP\_SEG}}{2} - T_{PROP(RxD,TxD)}\right)}{T_{PROP(BUS)}}$$

Where:

$L_{BUS\_MAX\_DEL}$ is the biggest allowed distance between any two nodes.

T_{PROP_SEG} is the length of PROP_SEG part of one bit period.

$T_{PROP(RxD,TxD)}$ is the propagation delay TxD to RxD of the used CAN transceiver.

$T_{PROP(BUS)}$ is the bus line delay per unit length.

Example

Given:

AMIS−42665 transceivers will be used with the following relevant parameters (extract from the datasheet):

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{pd(rec-dom)}$	Propagation Delay TxD to RxD		70	230	ns
$t_{pd(dom-rec)}$	Propagation Delay TxD to RxD		100	245	ns

The transceiver delay is slightly different for opposite edges (recessive to dominant vs. dominant to recessive). To analyze the worst case, we will take 245 ns.

The bus line has a delay of 5 ns per 1 m length

The bit rate of 500 kbps is required, resulting in 1 bit period of 2 μs

The CAN controller is setup to have PROP_SEG equal to 1100 ns

Then:

The maximum permissible bus line delay is (1100 ns / 2 – 245 ns) = 305 ns.

The maximum allowed distance between any two nodes $L_{BUS\_MAX\_DEL}$ is 61 m (= 305 ns / 5 ns).

Maximum Unterminated Stub Length

A CAN bus is intended to be as close as possible to a single line structure. However, deviations from this basic topology must be taken into account – e.g. for temporary connection of diagnostic equipment or for connection of nodes by short unterminated cables. In all these case, signal reflections will occur in the bus due to the existence of unterminated stubs. An example of a CAN bus with unterminated stubs can be seen in Figure 3.

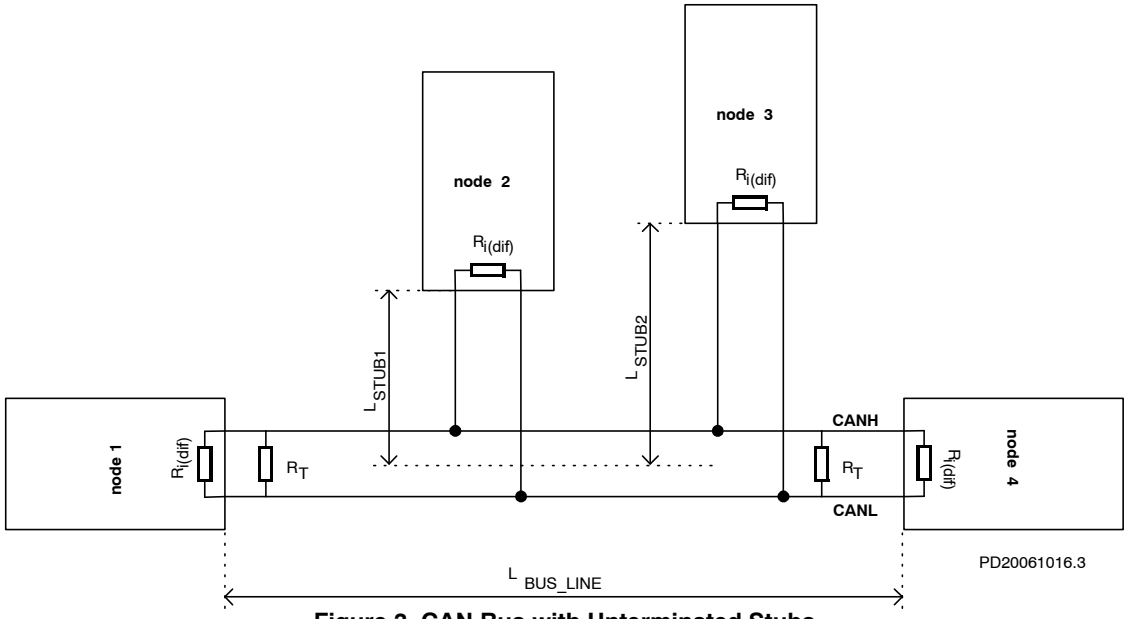

Figure 3. CAN Bus with Unterminated Stubs

Although the reflected signals will disappear once they arrive at a bus termination, and although the CAN protocol is robust, an upper limit must be set to the allowed unterminated stub length as well as to the cumulative stubs length.

Some rules of thumb can be used:

$$L_{STUB\_MAX} < \frac{T_{PROP\_SEG}}{50 \cdot T_{PROP(BUS)}}$$

AND

$$L_{STUB\_TOT\_MAX} < \frac{T_{PROP\_SEG}}{10 \cdot T_{PROP(BUS)}}$$

Where:

L_{STUB_MAX} is the maximum length of one unterminated stub.

$L_{STUB\_TOT\_MAX}$ is the cumulative length of all unterminated stubs in the bus.

T_{PROP_SEG} is the duration of the PROP_SEG part of the bit time (see the "Definition of CAN Bit Timing" section and Figure 1).

$T_{PROP(BUS)}$ is the propagation delay of the bus line per unit length.

Furthermore, the sum of all stub length must be subtracted from the maximum bus length $L_{BUS\_MAX\_DEL}$ calculated from the maximum permissible propagation delay (as per the "Definition of CAN Bit Timing" section). In the example depicted in Figure 3, the sum (L_{STUB1} + L_{STUB2} + L_{BUS_LINE}) must be less than $L_{BUS\_MAX\_DEL}$.

Example

Given:

AMIS−42665 transceivers will be used with the following relevant parameters (extract from the datasheet):

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD		70	230	ns
$t_{pd(dom-rec)}$	Propagation delay TxD to RxD		100	245	ns

The transceiver delay is slightly different for opposite edges (recessive to dominant vs. dominant to recessive). To analyze the worst case, we will take 245 ns.

Other parameters are:

The bus line has a delay of 5 ns per 1 m length

The bit rate of 500 kbps is required, resulting in 1 bit period of 2 μs

The CAN controller is setup to have PROP_SEG equal to 1100 ns

Then:

Maximum permissible stub length L_{STUB_MAX} is 4.4 m (1100 ns / 5 ns / 50)

Maximum permissible cumulative stub length $L_{STUB\_TOT\_MAX}$ is 22 m (1100 ns / 5 ns / 10)

If the full total length of stubs is used, the main bus line may be max. 39 m long (61 m – 22 m, see example in the "Maximum Unterminated Stub Length" section for $L_{BUS\_TOT\_MAX}$ calculation)

Maximum Bus Line Length in Function of the Required Signal Amplitude

Another limitation on the CAN bus topology is defined by the amplitude of the bus voltage required for correct reception of the bus state. Dominant bit signaled by any single node of the bus must be correctly detected as dominant at all other nodes. The signal amplitude is decreased by voltage drops along the bus line, as the bus is loaded by the bus terminations and the finite input resistances of the nodes. Signal integrity of a recessive state is not influenced by these drops, as it's defined by the termination resistors as typically zero differential voltage.

To analyze the effect of voltage drops, bus topology with n nodes shown in Figure 4 will be considered. A representation of the worst case is shown in Figure 5. The transmitting node, together with its termination resistor R_T, is placed on one side of the bus, whereas all other nodes and the second termination resistor are situated on the opposite side of the bus line. Each node loads the bus with its differential mode input resistance $R_{i(diff)}$, the non−zero resistance of the wires is represented by resistors R_W. The differential voltage driven by the transmitting node is denoted $V_{o(diff)}$, the receiving node can see differential voltage $V_{i(diff)}$ on its input.

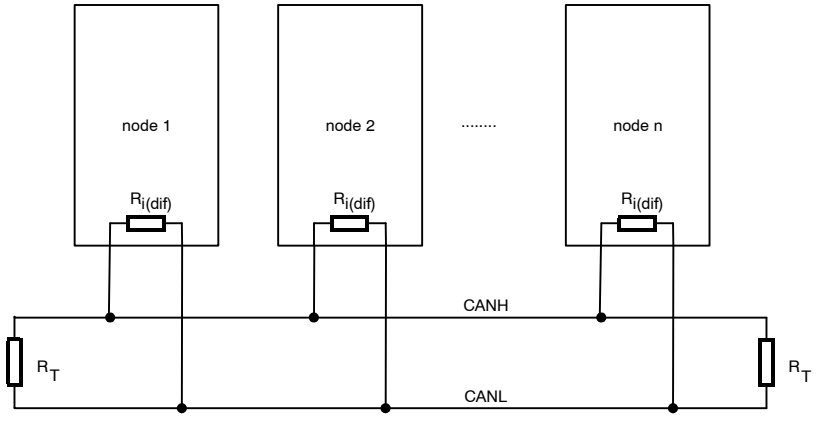

Figure 4. Basic CAN Bus Topology

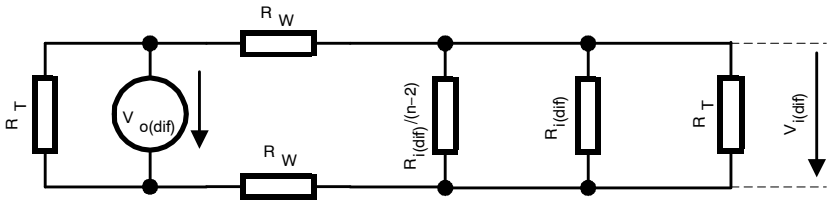

Figure 5. Electric Representation of the CAN bus from Figure 4

For proper detection of the dominant state, a minimum differential voltage $Vi_{(diff)\_MIN\_REQ}$ is required at the input of the receiving node. This minimum is given by the receiver threshold and a user−defined safety margin:

$$V_{i(diff)\_MIN\_REQ} = V_{i(diff)\_TH} + k \cdot \left(V_{o(diff)} - V_{i(diff)\_TH}\right)$$

Where:

$V_{i(diff)\_MIN\_REQ}$ is the minimum required dominant differential voltage at any receiving node

$V_{i(diff)\_TH}$ is the receiver threshold level

$V_{o(diff)}$ is the dominant differential voltage driven by the transmitting node

k is an optional “safety margin” coefficient, its value ranging from 0 to 1.

The maximum wire length with respect to the voltage drop can be then found out with the help of Figure 5 and considering following worst−case situation:

Minimum differential voltage $V_{o(diff)\_MIN}$ is driven by the transmitting node.

Maximum receiver threshold $V_{i(diff)\_MAX}$.

Maximum value of the bus resistance R_{W_MAX} is encountered.

Minimum termination resistors R_{T_MIN} are placed on the bus.

The nodes are loading the bus with their minimum differential input resistance $R_{i(diff)\_MIN}$.

Number of nodes connected to the bus is n_{NODES}.

Under the above conditions, the differential input voltage will reach its minimum:

$$V_{i(diff)\_MIN} = \frac{V_{o(diff)\_MIN}}{1 + 2.R_{W\_MAX} \cdot \left(\frac{1}{R_{T\_MIN}} + \frac{n_{NODES} - 1}{R_{i(diff)\_MIN}}\right)}$$

This worst case differential voltage must be higher than the required minimum $V_{i(diff)\_MIN\_REQ}$ defined above. Knowing that the cable resistance R_W is proportional to its length L with ratio ρ_W representing the specific resistance, both equations can be combined to yield:

$$L_{BUS\_MAX\_DROP} = \frac{1}{2.\rho_{W\_MAX}} \times \left\{ \frac{V_{o(diff)\_MIN}}{V_{i(diff)\_MAX} + k \cdot \left(V_{o(diff)\_MIN} - V_{i(diff)\_TH\_MAX}\right)} - 1 \right\} \times \frac{R_{T\_MIN} \cdot R_{i(diff)\_MIN}}{R_{i(diff)\_MIN} + \left(n_{NODES} - 1\right) \cdot R_{T\_MIN}}$$

Example

Given:

AMIS−42665 transceivers will be used with the following relevant parameters (extract from the datasheet):

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(dif)\ (bus\_dom)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0V; dominant; 42.5Ω < R_{LT} < 60Ω	1.5	2.25	3.0	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common−mode (see Figure 5)	−35V <V_{CANL} < +35V; −35V <V_{CANH} < +35V;	0.40	0.7	1.00	V
$R_{i(dif)}$	Differential input resistance		25	50	75	Ω

From the above table, the following inputs for the calculations will be extracted:

Minimum differential output voltage $V_{o(diff)\_MIN}$: 1.5 V

Maximum dominant threshold of the receiver $V_{i(diff)\_MAX}$: 1.00 V

Minimum differential input resistance of a receiver $R_{i(diff)\_MIN}$: 25000 Ω

Remaining inputs for the calculations are:

Maximum specific bus line resistance Q_{W_MAX}: 0.0346 Ω / m

Minimum termination resistor value R_{T_MIN}: 95 Ω

Number of nodes n_{NODES}: 60

Safety margin coefficient k: 0

Then:

Maximum bus line length with respect to the voltage drop is $L_{BUS\_MAX\_DROP}$: 560 m.

Maximum Number of Nodes in Function of the Transmitter Driving Capability

The maximum number of nodes is limited by the driving capability of a CAN transmitter. It's usually specified by the minimum allowed load resistance R_{L_MIN}. The load of a transmitter in the CAN bus is composed of the termination resistors and the parallel combination of differential input resistances of all nodes – see Figure 6.

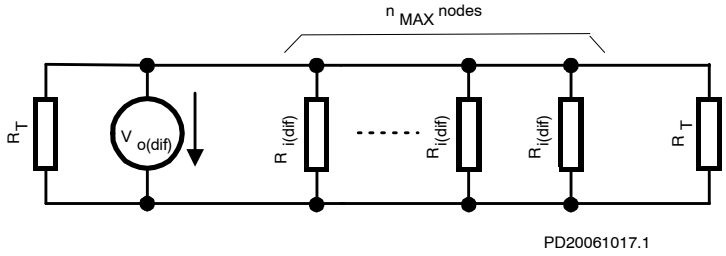

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Figure 6. Electric Representation of a CAN Bus for Calculation of the Maximum Number of Nodes

The transmitter is then loaded with resistance R_L, calculated as:

$$R_L = \frac{R_{T\_MIN} \times R_{i(diff)\_MIN}}{(n_{MAX} - 1) \times R_{T\_MIN} + 2 \cdot R_{i(diff)\_MIN}}$$

Where:

R_{T_MIN} is the minimum termination resistance.

$R_{i(diff)\_MIN}$ is the minimum differential input resistance of one node.

n_{MAX} is the number of nodes connected to the bus.

The resulting resistance R_L must stay above the specified minimum value R_{L_MIN}, leading to the following limit for the number of nodes:

$$n_{MAX} = 1 + R_{i(diff)\_MIN} \times \left(\frac{1}{R_{L\_MIN}} - \frac{2}{R_{T\_MIN}} \right)$$

Example

Given:

AMIS42665 transceivers will be used with the following relevant parameters (extract from the datasheet):

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(dif)\ (bus\_dom)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0V; dominant; 42.5 Ω < R_{LT} < 60 Ω	1.5	2.25	3.0	V
$R_{i(dif)}$	Differential input resistance		25	50	75	Ω

From the above table, the following inputs for the calculations will be extracted:
Minimum differential input resistance of a receiver $R_{i(diff)\_MIN}$: 25000 Ω.
Minimum allowed load to be driven by the transmitter R_{L_MIN}: 42.5 Ω (see the “Conditions” column of the above table).

Remaining input for the calculations is:
Minimum termination resistor R_{T_MIN}: 95 Ω

Then:
The maximum allowed number of nodes n_{MAX} connected to the CAN bus is 62.

References

[1] ISO11898/1 – Road vehicles – Controller area network (CAN) – Part 1: Data link layer and physical signaling

PUBLICATION ORDERING INFORMATION

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